

# ISDS205C User Guide

InstruStar Electronic Technology

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## **PC SYSTEM REQUIREMENTS**

- Windows XP, Win7, Win8, Win10
- Pentium or higher processor
- USB2.0 High speed port.
- 512MB RAM
- 1GB hard disk space

## 1.Introduction

ISDS205C dual-channel digital oscilloscope, with "low-cost, high-performance" as the design goals. well-designed bandwidth of 20M, 48M sampling rate, 2 channels, alternating support X-T and XY alternating pattern of two-channel virtual oscilloscope, spectrum analyzer, data recorder and logic analyzer. Logic analyzer support our Logic software and Saleae Logic 2 kinds of software, Saleae Logic supports SPI, IIC, UART, etc. 17 kinds protocol analysis. The device communicate with the PC via high speed USB2.0.

	Digital oscilloscope	Spectrum analyzers	Data recorder	Logic Analyzer
ISDS205C	√	√	√	√

## 2.Feature Description

Digital oscilloscope	
<b>Channels</b>	2
<b>Impedance</b>	1MΩ 25pF
<b>Coupling</b>	AC/DC
<b>Vertical resolution</b>	8Bit
<b>Gain range</b>	-6V ~ 6V (probe X1) -60V ~ 60V (probe X10)
<b>Vertical accuracy</b>	±3%
<b>Timebase range</b>	1ns-20s
<b>Input Protection</b>	Diode, 50Vpk
<b>Autoset</b>	Yes(10Hz to 20MHz)
<b>Trigger Mode</b>	Auto、 Normal and Signal
<b>Trigger Type</b>	No、 Rising edge、 Falling edge、 Rising edge or Falling edge
<b>Trigger level</b>	Yes
<b>Trigger Source</b>	CH1, CH2
<b>Buffer Size</b>	1MB/CH
<b>Bandwidth</b>	20MHz
<b>Max sample</b>	48MS/s
<b>Vertical mode</b>	CH1, CH2, ADD, SUB, MUL
<b>Display Mode</b>	X、 Y-T 和 X-Y
<b>measurements</b>	Yes
<b>Wave save</b>	Osc(Private)、 Excel and Bmp

Spectrum analyzers	
Channels	2
Bandwidth	20MHz
Algorithm	FFT(18 windows)、correlation
FFT points	8-1048576/CHN
FFT measure	Harmonic(1-7)、SNR、SINAD、ENOB、THD、SFDR
Filter processing	<p>FIR filter supports arbitrary range of frequency sampling method , and Rectangle, bartlett, triangular, cosine, hanning, bartlett_hanning, hamming, blackman, blackman_Harris, tukey, Nuttall, FlatTop, Bohman, Parzen, Lanczos, kaiser, gaussand dolph_chebyshev, window method design.</p> <p>IIR filter support "Butterworth", "Chebyshev I", "Chebyshev II", "Elliptic" type of filter design</p>

**Note: The oscilloscope factory calibration, if you are not satisfied with the measurements, can manual calibration, the specific reference oscilloscope instructions.**

Data recorder	
Channel	2
Impedance	1M $\Omega$ 25pF
Coupling	AC/DC
Vertical resolution	8Bit
Gain range	-6V ~ 6V (probe X1) -60V ~ 60V (probe X10)
Sample	1 channel : 1K~24M Hz 2 channel : 1K~16M Hz
Save File	The maximum 4G, recording time associated with the sampling rate

**Note: The specific speed recorder with computer processing speed, and if use high sampling rate, the situation may break.**

Logic Analyzer	
Channel	16
Sample	8 channel: 250K~24M Hz 16 channel: 250K~16M Hz
Sample points	1M-2GB

#### Saleae Logic Logic Analyzer

<b>Channel</b>	8
<b>Sample</b>	25K~24M Hz
<b>Protocol Analyzer</b>	Atmel SWI、BiSS C、SPI、I2C、CAN、UART、I2S/PCM、DMX-512、JTAG、LIN、Manchester、1-WIRE、UNI/O、Simple Parallel、MDIO、USB1.1、PS/2 Keyboard/Mouse
<b>Sample points</b>	1MB~10TB

### 3. Software Installation

Please refer to the "Software and Driver Installation.pdf".

### 4. Oscilloscope / Spectrum analyzer

Please refer to the "Multi VirAnalyzer User Guide.pdf", "Digital storage oscilloscope (Professional Version).pdf" and "Digital storage oscilloscope (Simplified Version).pdf".

### 5. Data Recorder

Please refer to the "Data Recorder.pdf".

### 6. Logic Analyzer

After the success of USB devices, data recoder, equipment selection drop-down combo box will appear ISDS205C(1.0) (N) option, choose a good future, the interface in Figure 6.1.

#### 6.1 Basic control

##### 6.1.1 Channel Control

Start or Stop Capture.

##### 6.1.2 Channel Num

Set the num of the channels to be collected.

##### 6.1.3 Sample Length

Set the length of the data to be collected.

##### 6.1.4 Sample

Select the speed of data collection.

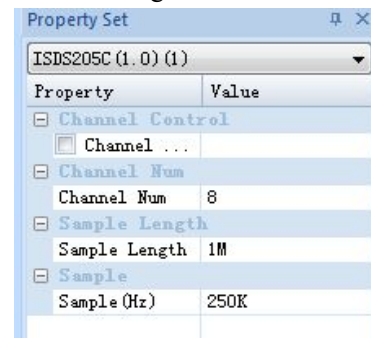


Figure 6.1 properties

#### 6.2 Record

Click the lower right corner "data record", the interface appears in Figure 6.2. Can display the recorded file. Double click the corresponding file, you can load, view the collected data.

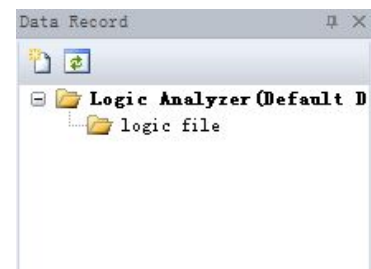


Figure 6.2 data record

### 7. Saleae Logic logic analyzer

The device to support Saleae Logic software, the development of the hardware above appropriated Saleae Logic position. Plugged into the USB, the software automatically recognizes and displays the Connected. Interface shown in Figure 7.1

More information, please view Saleae Logic software instructions, is located in "\Saleae Logic\Logic Guide.pdf"

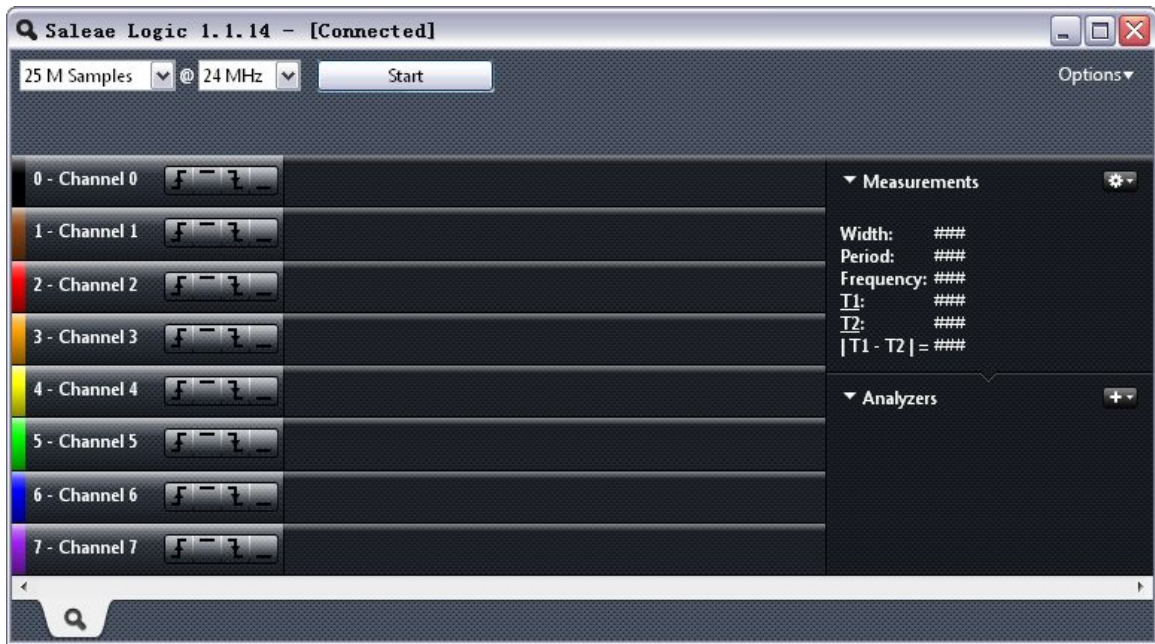


Figure 7.1 Saleae Logic interface